REMARKS/ARGUMENTS

The applicant's attorneys appreciate the Examiner's thorough search and remarks.

Claims 1 and 25 have been rejected as obvious over Fujishima in view of Nakagawa. Reconsideration is requested.

Claim 1 calls for the following combinations:

1. A semiconductor device comprising:

a semiconductor substrate of a first conductivity;

an epitaxially formed semiconductor layer of a second conductivity formed over said substrate;

a body region of said first conductivity formed in said epitaxially formed semiconductor layer;

a source region of said second conductivity formed in said body region, said source region being adjacent an invertible channel in said body region;

a gate structure formed over said invertible channel region, said gate structure including a gate electrode which is spaced from said invertible channel by a gate insulation layer;

a drain region formed in said epitaxially formed semiconductor layer, said drain region and said body region being spaced from one another by a drift region in said epitaxially formed semiconductor layer;

a resurf region of said first conductivity formed in said epitaxially formed semiconductor layer, said resurf region being formed over at least a portion of said drift region; and

a field plate structure disposed over said resurf region, said field plate structure including a first field plate disposed over a first insulation layer of a first thickness, a second field plate disposed over a second insulation layer of a second thickness, said second insulation layer being formed over said first insulation layer, and a third field plate spaced from said second field plate by a third insulation layer of a third thickness, wherein said first field plate includes a first portion spaced from a second portion by a first gap, said second field plate includes a first portion spaced from a second portion by a second gap, and said

third field plate includes a first portion spaced form a second portion by a third gap, and wherein said first gap is wider than said second gap and said third gap, and said second gap is wider than said third gap, and wherein said gaps are filled only with an insulation material.

Claim 25 call for the following combination:

25. A field plate structure comprising:

a first field plate;

a second field plate disposed above and spaced from said first field plate; and

a third field plate disposed above and spaced from said second field plate,

said field plate structure being disposed over a resurf region, wherein said first field plate includes a first portion spaced from a second portion by a first gap, said second field plate includes a first portion spaced from a second portion by a second gap, and said third field plate includes a first portion spaced form a second portion by a third gap, and wherein said first gap is wider than said second gap and said third gap, and said second gap is wider than said third gap, and wherein said gaps are filled only with an insulation material.

Claims 1 and 25 now call for the gaps between the first and second portion of the field plates to be filled only with an insulation material. On the other hand, Nakagawa teaches the use of floating conductive elements 13, 13′ as a required part of its structure to shield region 5 from field plates 8′ and 9′:

> Together with the floating conductive elements 13 and 13′, the field plates 8′ and 9′ function to completely cover the N-type high resistance layer 5 so that reliability of the MOS transistor is improved. Further, the two or more floating conductive elements as indicated by 13 and 13′ electrically shield the N-type pinch high resistance layer 5 from influence by the field plates 8′ and 9′ so that good properties in sustaining the voltage for the transistor are obtained. Col. 3, lines 3-11.

Nakagawa does not suggest that the floating conductive elements can be eliminated from the structure.

Furthermore, Claim 1 calls for the field plate structure to be disposed over a resurf region. The resurf region is of the same conductivity as the base region of the device, i.e. the first conductivity. On the other hand, Nakagawa teaches a field plate structure overlying an N-type, pinch or high resistance region 5, which is of a conductivity that is opposite to the P-type base region 4. Moreover, there is no suggestion that any part of the field plate of Nakagawa can be readily incorporated into a device in which the resurf region is the same conductivity as the channel region.

In addition, there is no teaching or suggestion for a skilled person to select portion 14 out of the Nakagawa device and incorporate the same into the device shown by Fujishima. That is, absent the inventor's disclosure, one skilled in the art would not be led to only pick portion 14 of Nakagawa to modify Fujishima.

For the above reasons, it is respectfully suggested that claims 1 and 25 are not obvious over the art of record. Reconsideration is requested.

The application is believed to be in condition for allowance. Such action is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 8, 2006:

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Signature

May 8, 2006
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Respectfully submitted,

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